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## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

H. Bernhard Pogge et al.

Examiner: Not yet assigned

Application No.: Not yet assigned

Group Art Unit: 2812

Filed: Herewith

For: PROCESS FOR MAKING FINE

> PITCH CONNECTIONS BETWEEN **DEVICES AND STRUCTURE**

MADE BY THE PROCESS

Date: June 25, 2003

EXPRESS MAIL NO. 5070 225875005 I HEREBY CERTIFY THAT THIS CORRESPONDENCE IS BEING DEPOSITED WITH THE U.S. POSTAL SERVICE AS EXPRESS MAIL IN AN ENVELOPE ADDRESSED TO: COMMISSIONER OF PATENTS AND TRADEMARKS, WASHINGTON, D.C. 20231

APPLICANT AND/OR ATTORNEY REQUESTS THE DATE OF DEPOSIT AS THE FILE DATE

DATE OF DEPOSIT

PRELIMINARY AMENDMENT

The Commissioner for Patents Washington, D.C. 20231

This application is a division

of Application No. 10/213,872

under 37 C.F.R. § 1.53(b)

filed August 6, 2002

Sir:

Prior to examination on the merits, please amend the above-identified application as follows:

FIS9-2000-0134-US3

## AMENDMENTS TO THE CLAIMS

Claims 1-16 (cancelled)

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Claim 17 (original): A semiconductor device including a plurality of chips, the chips having front surfaces and back surfaces, the device comprising:

a support attached to the chips on the back surfaces thereof;

a first layer disposed on the front surfaces of the chips and having a plurality of vias formed therein and conducting pads in registration with the vias;

a phirality of studs corresponding to the vias and disposed therein; and

a second layer attached to the first layer on a surface of the first layer opposite the front surfaces of the chips, the second layer being aligned to the first layer by the studs in the vias, the second layer including electrical wiring connecting to the chips through the studs and the conducting pads,

wherein said plurality of chips includes chips with active devices and a chip without active devices.

- Claim 18 (original): A semiconductor device according to claim 17, further comprising an attachment layer between the support and the chips, wherein the attachment layer has a plurality of support connection vias formed therein, support connection pads in registration with the support connection vias, and a plurality of support connection studs disposed in the support connection vias and connected to the support connection pads.
- Claim 19 (original): A semiconductor device according to claim 17, wherein the chip without 1 active devices has passive components fabricated thereon. 2
- Claim 20 (original): A semiconductor device according to claim 17, wherein the chip without 1 active devices has a size according to a placement pattern of the chips with active devices. 2

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## REMARKS

This application is a division under 37 C.F.R. § 1.53(b) of Application No. 10/213,872, filed August 6, 2002.

Claims 17-20 are now presented for examination. Claims 1-16 have been cancelled without prejudice. Claim 17 is the only independent claim. Favorable review is respectfully requested.

It is noted that claims 1-20 of the prior application were subject to a restriction requirement (Office Action dated April 29, 2003). Claims 1-16 of that application were elected for prosecution on the merits. Claims 17-20 presented herewith are identical to the claims directed to the non-elected invention in the prior application.

In view of the foregoing amendments and remarks, the applicants respectfully request favorable consideration and early passage to issue of the present application.

The applicants' undersigned attorney may be reached by telephone at (845) 894-3667. All correspondence should continue to be directed to the below listed address.

Respectfully submitted,

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